Remarks/Arguments:

In the specification, Applicant inadvertently submitted an incorrect filing date in the reference to the benefit claim to prior filed application no. 10/390,254. The USPTO recognized the priority claim and listed the filing date correctly on the Filing Receipt, pointing out that the data provided by the Applicant is not consistent with that of the PTO records. The section entitled, "Cross Reference To Related Applications: has been amended to correct the filing date of prior filed application no. 10/390,254.

Claims 1-3, 5, 7-14, as amended and new claims 15-16 are presented for consideration.

The Examiner rejects claims 1-3 and 8-11 under 35 U.S.C. 102 as anticipated by the disclosures in published U.S. patent application no. 2003/0189202, filed by Li et al (the "Li PPA").

The Examiner rejects claims 4-7 and 11-13 under 35 U.S.C. 103(a) as obvious in view of the combined disclosures in the Li PPA, published U.S. patent application no. 2004/0071951, filed by Jin (the "Jin PPA"), and published U.S. patent application no. 2001/0030366, filed by Nakano et al (the "Nakano PPA"). Claim 14, dependent upon claim 1, was also presented as part of the original filing. For purposes of efficiency, the Applicants will treat the Section 103(a) rejection as also covering claim 14 in this response.

The Li PPA discloses methods for fabrication of nanowire devices in which: (1) one or more electrodes is set down on a conducting substrate; (2) a pattern of one or more nanowire growth catalyst sites is provided on each electrode; (3) one or more nanowires is grown on each catalyst site; (4) each nanowire is connected to a selected electrical source at an "exposed end" of the nanowire; (5) each nanowire is surrounded by interstitial electrical insulation, extending between adjacent nanowires, to insulate the nanowires from each other;

(6) each nanowire is planarized at an exposed end to expose a tip of a nanowire above the insulation material (Figures 4a-4f).

The Jin PPA discloses a high density information storage medium and fabrication method, which uses a periodic array of vertically aligned carbon nanotubes ("CNTs") for such storage. Each CNT is coated with, or filled with, a selected magnetic material (Fe, Ni, Co), interstitial gaps between adjacent coated CNTs are filled with a non-magnetic material, such as a metal or alloy (Al, Ti, Si, Cu, Mo or Cr or alloy thereof) and the array of coated CNTs and gap material are planarized to expose tips of the coated or filled CNTs (Figure 3). Optionally, as indicated in Figures 5B and 5C, the nanowire surfaces are oxidized, and subsequently subjected to a reducing atmosphere.

The Nakano PPA discloses a method for producing a semiconducting system, using a protective coating of TaN or TiN.

Amended claim 1 recites a method for fabricating an electrical connection, the method comprising:

providing an electrically non-conductive layer of a first selected material, having a first selected thickness, on an exposed surface of a substrate of selected substrate material;

providing an electrically conductive layer of a second selected material, having a second selected thickness, in a first selected pattern having at least first and second spaced apart conductive layer components, on an exposed surface of the non-conductive layer;

depositing an array, including at least first and second spaced apart catalyst array elements, of metallic nanowire ("MeNW") catalyst material of a selected catalyst thickness on the conductive layer so that the at least first and second catalyst array elements lie on the respective first and second conductive layer components;

providing a gas or vapor of a selected metallic or organometallic material around the catalyst array, and allowing at least first and second MeNWs to grow,

substantially perpendicular to a plane P of the conductive layer on the respective first and second conductive layer components;

providing a diffusion barrier of a selected barrier material as a thin coating surrounding a side wall of the at least two MeNWs and surrounding the exposed portions of the conductive layer, to prevent migration of the MeNW material;

depositing an insulation layer of a selected insulation material over an exposed surface of the conductive layer and around the at least two MeNWs so that an interstitial region between at least two adjacent MeNWs contains the insulation material; and

applying a chemical mechanical polishing process or etching process to remove a fraction of each of the at least two MeNWs, and a fraction of the insulation layer so that each of the at least two MeNWs has an end exposed.

Amended claim 1 recites provision of a diffusion barrier, which may be conductive or non-conductive, as a thin coating surrounding a side wall of (spaced apart) MeNWs and surrounding exposed portions of the conductive layer, to prevent migration of the MeNW material.

. Use of a diffusion barrier for such purpose is discussed on page 4, lines 1-5, of the specification. Provision of the diffusion layer serves as a barrier to migration of metal-like substances from the MeNWs into or through an interstitial insulation layer surrounding the MeNWs and permits isolation of a first signal intended for one array element (e.g., the first array element) from a second signal intended for another array element (e.g., the second array element).

None of the Li PPA, the Jin PPA and the Nakano PPA (referred to collectively herein as the "cited references") discloses provision of one or more diffusion barriers as a thin coating for the MeNWs, to suppress electro-migration from the MeNWs. The Li PPA discloses use of individual pads 14 for isolated electrical addressing. The Jin PPA uses only a non-isolated, continuous substrate 11 as the base for nanowire-based nanomagnets, and hence does not provide individual electrical addressing. The Jin PPA uses the magnetic properties of nanostructures having magnetic coatings, which are embedded in interstitial filler

(conductive) metal that is non-magnetic. The nanotube coating 13 disclosed in the Jin PPA is a magnetic material (Fe, Ni, Co), not a general material as recited in claim 1, and is used in the Jin PPA to enhance magnetic performance of the nanotube recording medium 12, as discussed in connection with Figure 3B. The Nakano PPA is concerned with semiconductor fabrication, not with addressing or suppressing migration between nanostructures.

Amended claim 1 recites use of a patterned conductive layer to suppress electrical current between isolated elements and requires use of non-conductive interstitial filler, plus a thin, robust barrier coating of general material for isolating and confining migration of the MeNW material. It would not have been obvious, from the combined disclosures of the Li PPA, the Jin PPA and the Nakano PPA, to provide a thin diffusion barrier of general material, surrounding each MeNW, to suppress electro-migration from or between adjacent MeNWs and to electrically isolate spaced apart portions of catalyst array elements from each other, as recited in amended claim 1.

The Applicants believe that amended claim 1, and claims 2-3, 5 and 7-16 dependent thereon, as amended, are allowable over, and are not anticipated by or made obvious in view of, the individual or combined disclosures of the Li PPA, the Jin PPA and the Nakano PPA. The Applicants request that the Examiner pass the application, including claims 1-3, 5 and 7-16, as amended, to issue as a U.S. patent.

Respectfully submitted,

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Date

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